WHAT IS CLAIMED IS:

1. A gate voltage regulation system for the programming and/or soft programming phase of non volatile memory cells, wherein the memory cells being organized in cell matrices with corresponding circuits responsible for addressing, decoding, reading, writing and erasing the memory cell content, comprising:

charge pump voltage regulators for biasing gate terminals of the cells in the programming phase with a predetermined voltage value;

a first regulation stage and a second regulation stage, being structurally independent, responsible for the programming phase and soft programming phase, respectively, the first stage generating a supply voltage for said second stage.

2. The system according to claim 1, wherein said second stage comprises a current mirror structure with an output stage comprising a transistor.

3. The system according to claim 2, wherein a circuit branch of said current mirror structure comprises a current mirror structure disabling transistor controlled by a switching signal in correspondence with said programming phase.

4. The system according to claim 3, wherein said structure disabling transistor of said current mirror structure operates in a saturation status.

5. The system according to claim 1, wherein said first stage comprises a charge pump supplied with a supply voltage and regulated by means of a stable voltage regulator.

6. The system according to claim 1, wherein an output of said second stage is coupled to the gate terminals of the cells.

7. A circuit, comprising:

a first voltage regulation stage that generates a voltage ramp output at a first output;

a second voltage regulation stage that generates a regulated voltage output at a second output; and

a selection switch that responds to a control signal to selectively connect the first output to the second output.

8. The circuit as in claim 7 wherein the second output is coupled to gate terminals of a plurality of volatile memory cells.

9. The circuit as in claim 8 wherein the control signal has a first value which activates the selection switch to apply the voltage ramp output to the gate terminals of the plurality of memory cells, and a second value which de-activates the selection switch to apply the regulated voltage output to the gate terminals of the plurality of memory cells.

10. The circuit as in claim 9 wherein the control signal first value causes a programming of the plurality of memory cells and the control signal second value causes a soft programming of the plurality of memory cells.

11. The circuit as in claim 7 wherein the first output of the first voltage regulation stage is a power supply for the second voltage regulation stage.

12. The circuit as in claim 7 wherein the second output is coupled to gate terminals of a plurality of floating gate memory cells.

13. A circuit, comprising:

a plurality of volatile memory cells, each including a transistor, each of the transistors sharing a common gate connection; and

a gate voltage regulator circuit having an output coupled to the common gate connection and receiving a programming control signal, the gate voltage regulator circuit comprising:

a first regulator generating a programming ramp voltage;

a second regulator generating a soft programming voltage; and

a selection circuit responsive to the programming control signal for applying the programming ramp voltage to the common gate connection in a first operating mode and applying only the soft programming voltage to the common gate connection in a second operating mode.

14. The circuit of claim 13:

wherein the first regulator has a first output at which the programming ramp voltage is generated;

where in the second regulator has a second output at which the soft programming voltage is generated, and which is coupled to the common gate connection; and

wherein the selection circuit comprises a switching circuit that selectively connects the first output to the second output.

15. The circuit of claim 14 wherein then switching circuit comprises a transistor having its conduction terminal coupled between the first and second outputs and its control terminal coupled to receive the programming control signal.

16. The circuit of claim 13 wherein the first regulator has a first output at which the programming ramp voltage is generated and wherein the first output of the first regulator is a power supply for the second regulator.

17. The circuit of claim 13 wherein the transistor of each volatile memory cell is a floating gate transistor.

18. The circuit of claim 13 wherein the selection circuit absorbs voltage changes in the programming ramp voltage when in the second operating mode so as to allow a substantially constant current to be supplied with the soft programming voltage.

19. The circuit of claim 18 wherein the selection circuit permits voltage changes in the programming ramp voltage to be applied to the common gate connection when in the second operating mode.